CAD Algorithms for Physical Design - Netlist Hierarchy and Connectivity Representation

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Contents

- Verilog Hierarchy
- Alternative Representations
  - Gatepin-level Connectivity (Direct)
  - Net-based Connectivity (Indirect)

Wire ≡ Net ≡ input/output

Hierarchical Netlist Example

counter-MAPPED7.v

```
module counter_DW01_inc_0 ( A, SUM );
  input [7:0] A;
  output [7:0] SUM;
  wire   [7:2] carry;

  adhalf_1 U1_1_6 ( .a(A[6]), .b(carry[6]), .co(carry[7]), .s(SUM[6]) );
  adhalf_1 U1_1_1 ( .a(A[1]), .b(A[0]), .co(carry[2]), .s(SUM[1]) );
  adhalf_1 U1_1_2 ( .a(A[2]), .b(carry[2]), .co(carry[3]), .s(SUM[2]) );
  adhalf_1 U1_1_3 ( .a(A[3]), .b(carry[3]), .co(carry[4]), .s(SUM[3]) );
  adhalf_1 U1_1_4 ( .a(A[4]), .b(carry[4]), .co(carry[5]), .s(SUM[4]) );
  adhalf_1 U1_1_5 ( .a(A[5]), .b(carry[5]), .co(carry[6]), .s(SUM[5]) );
  inv_2 U1 ( .a(A[0]), .x(SUM[0]) );
  exor2_1 U2 ( .a(carry[7]), .b(A[7]), .x(SUM[7]) );
endmodule

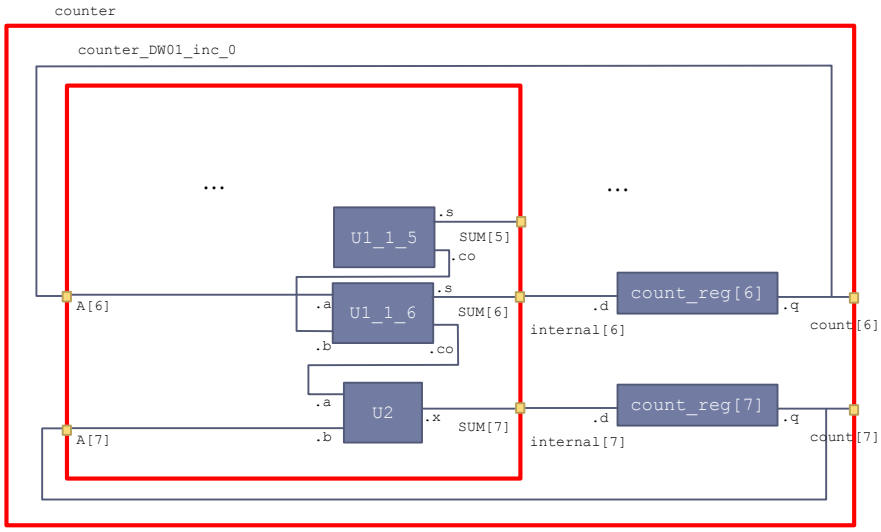
module counter ( clk, reset, count );
  output [7:0] count;
  input clk, reset;
   wire [7:0] internal;
  wire  n18;

  counter_DW01_inc_0 add_13 ( .A(count), .SUM(internal[7:0])); // not multinet - {} //
  dffpr_2 \count_reg[7]  ( .d(internal[7]), .ck(clk), .rb(n18), .q(count[7]) );
  dffpr_2 \count_reg[4]  ( .d(internal[4]), .ck(clk), .rb(n18), .q(count[4]) );
  dffpr_2 \count_reg[5]  ( .d(internal[5]), .ck(clk), .rb(n18), .q(count[5]) );
  dffpr_2 \count_reg[6]  ( .d(internal[6]), .ck(clk), .rb(n18), .q(count[6]) );
  dffpr_2 \count_reg[2]  ( .d(internal[2]), .ck(clk), .rb(n18), .q(count[2]) );
  dffpr_2 \count_reg[3]  ( .d(internal[3]), .ck(clk), .rb(n18), .q(count[3]) );
  dffpr_2 \count_reg[1]  ( .d(internal[1]), .ck(clk), .rb(n18), .q(count[1]) );
  dffpr_2 \count_reg[0]  ( .d(internal[0]), .ck(clk), .rb(n18), .q(count[0]) );
  inv_2 U4 ( .a(reset), .x(n18) );
endmodule
```

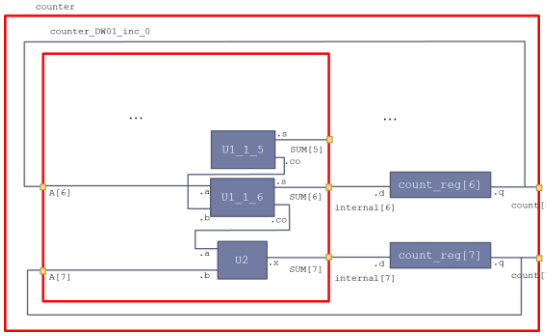

Gatepin-Level Connectivity Representation

- No Nets/Wires stored, only gatepin to gatepin connections
  - Similar to a graph representation where gatepins are nodes
- Gatepin
  - Each gatepin is connected to a list of gatepins
  - Its connected gatepins may be Module I/O gatepins
- Simple Representation
- Redundancy
  - As connections of a→b are stored both in a and in b

Partial Schematic



Gatepin-based Connectivity



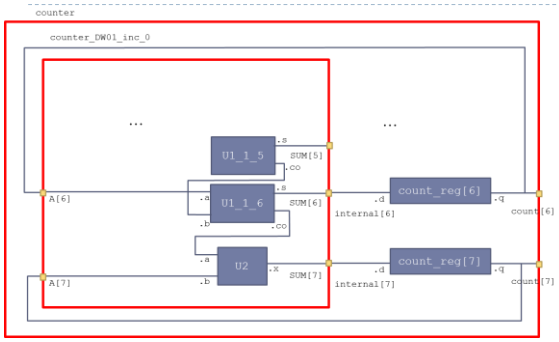
Gatepins:

```
Gate Pin: counter_DW01_inc_0/A|7
Connections: (4)
counter_DW01_inc_0/U2/b (no delay info)
counter/count|7 (no delay info)
counter/add_13/A|7 (no delay info)
counter/\count_reg[7]/q (no delay info)
----------------------------------------
Gate Pin: counter_DW01_inc_0/SUM|7
Connections: (3)
counter_DW01_inc_0/U2/x (no delay info)
counter/add_13/SUM|7 (no delay info)
counter/\count_reg[7]/d (no delay info)
----------------------------------------
Gate Pin: counter/\count_reg[7]/d
Connections: (2)
counter/add_13/SUM|7 (no delay info)
counter_DW01_inc_0/SUM|7 (no delay info)
----------------------------------------
Gate Pin: counter/count|7
Connections: (3)
counter/add_13/A|7 (no delay info)
counter_DW01_inc_0/A|7 (no delay info)
counter/\count_reg[7]/q (no delay info)
----------------------------------------
Gate Pin: counter_DW01_inc_0/U1_1_6/co
Connections: (1)
counter_DW01_inc_0/U2/a (no delay info)
----------------------------------------
Gate Pin: counter/\count_reg[7]/q
Connections: (3)
counter/count|7 (no delay info)
counter/add_13/A|7 (no delay info)
counter_DW01_inc_0/A|7 (no delay info)
```

- Tracing Gatepin `counter/count_reg[7]/q` connections?
- Tracing Gatepin `counter/count_reg[7]/d` connections?

Gatepin-based Connectivity

Gatepins:

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Gate Pin: counter_DW01_inc_0/U1_1_6/co
Connections: (1)
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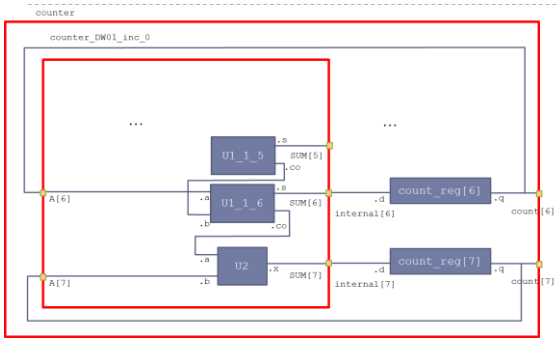
Connections: (3)
counter/count|7 (no delay info)
counter/add_13/A|7 (no delay info)
counter_DW01_inc_0/A|7 (no delay info)
```

Connected gatepins

- Tracing Gatepin `counter/count_reg[7]/q` connections?
- Tracing Gatepin `counter/count_reg[7]/d` connections?

Gatepin-based Connectivity

Gatepins:

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Connections: (3)
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Gate Pin: counter_DW01_inc_0/U1_1_6/co
Connections: (1)
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----------------------------------------
Gate Pin: counter/\count_reg[7]/q
Connections: (3)
counter/count|7 (no delay info)
counter/add_13/A|7 (no delay info)
counter_DW01_inc_0/A|7 (no delay info)
```

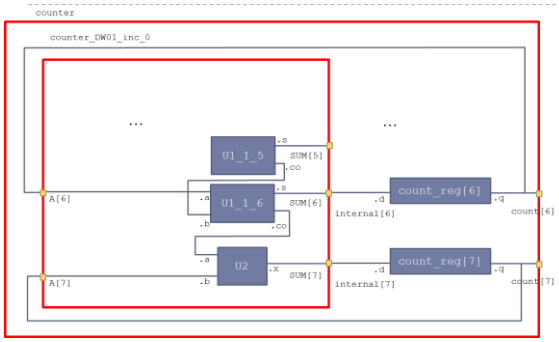
Next level of Connected gatepins

Connected gatepins

- Tracing Gatepin `counter/count_reg[7]/q` connections?
- Tracing Gatepin `counter/count_reg[7]/d` connections?

Gatepin-based Connectivity

Gatepins:

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Gate Pin: counter/\count_reg[7]/d
Connections: (2)
counter/add_13/SUM|7 (no delay info)
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----------------------------------------
Gate Pin: counter/count|7
Connections: (3)
counter/add_13/A|7 (no delay info)
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Gate Pin: counter_DW01_inc_0/U1_1_6/co
Connections: (1)
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Gate Pin: counter/\count_reg[7]/q
Connections: (3)
counter/count|7 (no delay info)
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counter_DW01_inc_0/A|7 (no delay info)
```

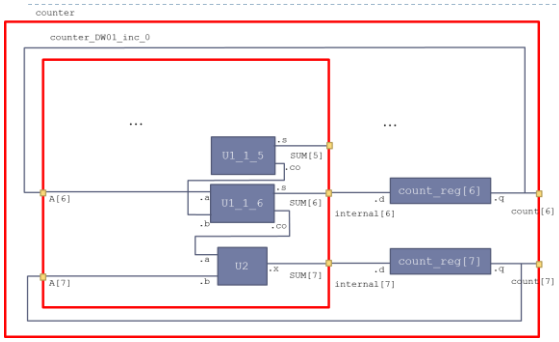
Connected gatepins

- Tracing Gatepin `counter/count_reg[7]/q` connections?
- Tracing Gatepin `counter/count_reg[7]/d` connections?

Gatepin-based Connectivity

Gatepins:

Next level of Connected gatepins

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Gate Pin: counter/\count_reg[7]/q
Connections: (3)
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counter_DW01_inc_0/A|7 (no delay info)
```

Connected gatepins

- Tracing Gatepin `counter/count_reg[7]/q` connections?
- Tracing Gatepin `counter/count_reg[7]/d` connections?

Net-based Connectivity Representation

- Net
  - A net is a list of gatepins
  - A net may also be a gatepin itself
    - When it is a module I/O
  - Module I/O gatepin nets are updated
    - When new modules, new wires and instances are declared
- Gatepin
  - Each Gatepin is related to a single Net
  - the associated Net may itself be a gatepin - Module I/O port gatepin
  - The list of gatepins in its net
    - Are connected gatepins at this level of the hierarchy
    - The connected gatepins may also be themselves be nets
      - As they may be Module I/O pins down of up in the hierarchy

Net-based Connectivity Representation

- Net updating
  - In net-based connectivity gatepin nets must be replaced when a new level of hierarchy is introduced:

Net Replacements for Example

```
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/SUM|6 (was counter_DW01_inc_0/SUM|6) with counter/internal|6
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/SUM|7 (was counter_DW01_inc_0/SUM|7) with counter/internal|7
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/SUM|4 (was counter_DW01_inc_0/SUM|4) with counter/internal|4
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/SUM|5 (was counter_DW01_inc_0/SUM|5) with counter/internal|5
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/SUM|2 (was counter_DW01_inc_0/SUM|2) with counter/internal|2
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/SUM|3 (was counter_DW01_inc_0/SUM|3) with counter/internal|3
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/SUM|0 (was counter_DW01_inc_0/SUM|0) with counter/internal|0
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/SUM|1 (was counter_DW01_inc_0/SUM|1) with counter/internal|1
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/A|2 (was counter_DW01_inc_0/A|2) with counter/count|2
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/A|3 (was counter_DW01_inc_0/A|3) with counter/count|3
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/A|0 (was counter_DW01_inc_0/A|0) with counter/count|0
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/A|1 (was counter_DW01_inc_0/A|1) with counter/count|1
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/A|6 (was counter_DW01_inc_0/A|6) with counter/count|6
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/A|7 (was counter_DW01_inc_0/A|7) with counter/count|7
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/A|4 (was counter_DW01_inc_0/A|4) with counter/count|4
DEBUG: Replacing Original Net of Gatepin counter_DW01_inc_0/A|5 (was counter_DW01_inc_0/A|5) with counter/count|5
```

Net-based Connectivity Representation

- Net updating
  - In net-based connectivity gatepin nets must be replaced when a new level of hierarchy is introduced:

Gatepin
`counter_DW01_inc_0/SUM|7`
before net replacement:

```
---------------------------------------
Gate Pin: counter_DW01_inc_0/SUM|7
Connections: (0)
(Module counter_DW01_inc_0)
NONE.
Net Connection: counter_DW01_inc_0/SUM|7
(Net) Connections (1):
counter_DW01_inc_0/U2/x
---------------------------------------
```

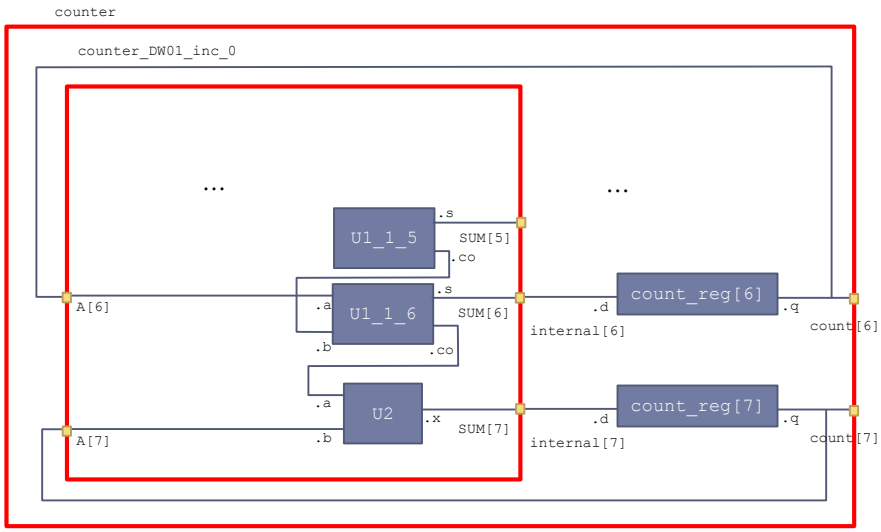
Gatepin
`counter_DW01_inc_0/SUM|7`
after net replacement:

```
---------------------------------------
Gate Pin: counter_DW01_inc_0/SUM|7
Connections: (0)
(Module counter_DW01_inc_0)
NONE.
Net Connection: counter/internal|7
(Net) Connections (3):
counter/add_13/SUM|7
counter_DW01_inc_0/SUM|7
counter/\count_reg[7]/d
---------------------------------------
```

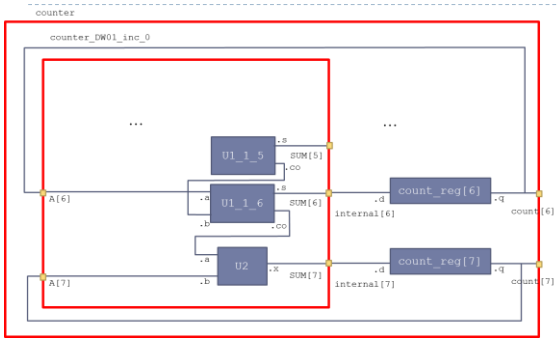
  - Net itself is not modified:

```
---------------------------------------
Net Name: counter_DW01_inc_0/SUM|7
Connections (1):
counter_DW01_inc_0/U2/x
---------------------------------------
```


Partial Schematic



Net-based Connectivity

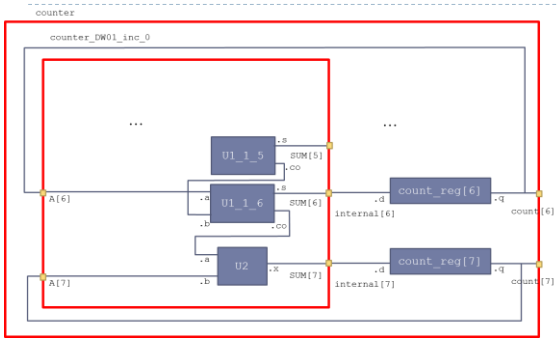


Nets:

```
Net Name: counter_DW01_inc_0/A|7
Connections (1):
counter_DW01_inc_0/U2/b
----------------------------------------
Net Name: counter_DW01_inc_0/SUM|7
Connections (1):
counter_DW01_inc_0/U2/x
----------------------------------------
Net Name: counter/internal|7
Connections (3):
counter/add_13/SUM|7
counter_DW01_inc_0/SUM|7
counter/\count_reg[7]/d
----------------------------------------
Net Name: counter/count|7
Connections (3):
counter/add_13/A|7
counter_DW01_inc_0/A|7
counter/\count_reg[7]/q
----------------------------------------
Net Name: counter_DW01_inc_0/carry|7
Connections (2):
counter_DW01_inc_0/U1_1_6/co
counter_DW01_inc_0/U2/a
```

- Tracing Gatepin `counter/count_reg[7]/q` connections?
  - Net connection ➔ `count[7]`
- Tracing Gatepin `counter/count_reg[7]/d` connections?
  - Net connection ➔ `internal[7]`

Net-based Connectivity



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counter/add_13/SUM|7
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Net Name: counter/count|7
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Net Name: counter_DW01_inc_0/carry|7
Connections (2):
counter_DW01_inc_0/U1_1_6/co
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Net gatepins

- Tracing Gatepin `counter/count_reg[7]/q` connections?
  - Net connection ➔ `count[7]`
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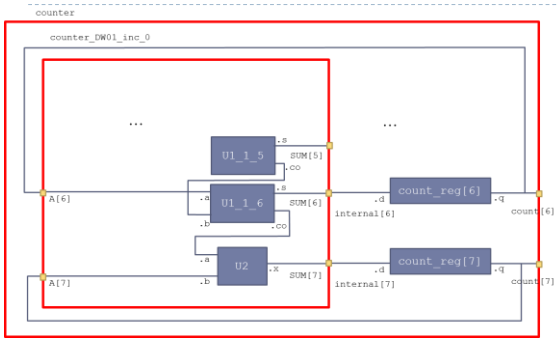
Net-based Connectivity



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Gatepin is also a Net

Net gatepins

- Tracing Gatepin `counter/count_reg[7]/q` connections?
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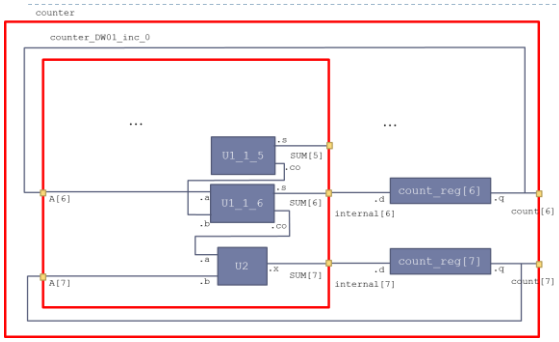

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counter/\count_reg[7]/d
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Net Name: counter/count|7
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counter/\count_reg[7]/q
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Gatepin is also a Net

Net gatepins

- Tracing Gatepin `counter/count_reg[7]/q` connections?
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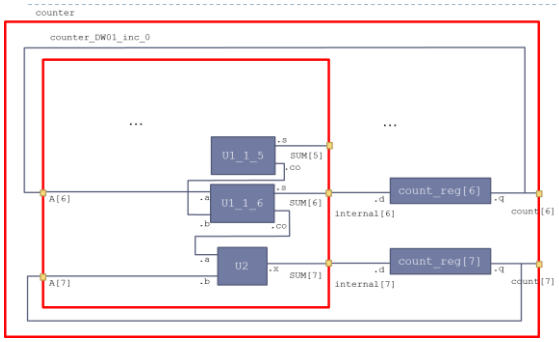

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Connections (1):
counter_DW01_inc_0/U2/x
-----------------------------------------
Net Name: counter/internal|7
Connections (3):
counter/add_13/SUM|7
counter_DW01_inc_0/SUM|7
counter/\count_reg[7]/d
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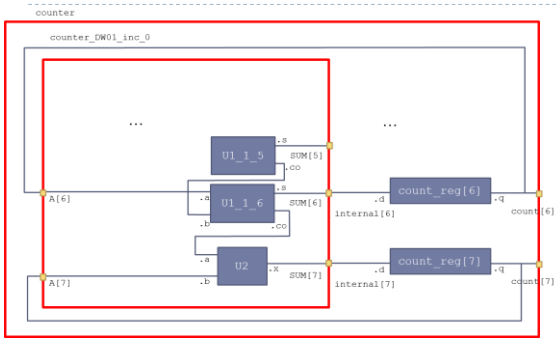
Net Name: counter/count|7
Connections (3):
counter/add_13/A|7
counter_DW01_inc_0/A|7
counter/\count_reg[7]/q
-----------------------------------------
Net Name: counter_DW01_inc_0/carry|7
Connections (2):
counter_DW01_inc_0/U1_1_6/co
counter_DW01_inc_0/U2/a
```

Net gatepins

- Tracing Gatepin `counter/count_reg[7]/q` connections?
  - Net connection ➔ `count[7]`
- Tracing Gatepin `counter/count_reg[7]/d` connections?
  - Net connection ➔ `internal[7]`

Net-based Connectivity



Nets:

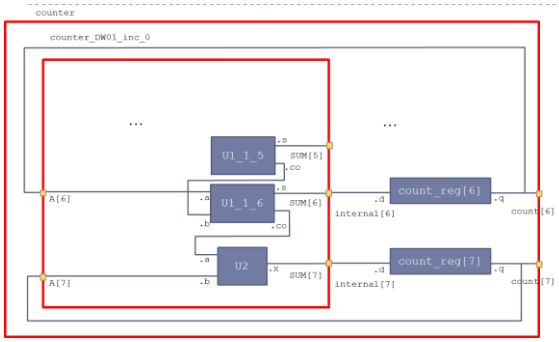
```
Net Name: counter_DW01_inc_0/A|7
Connections (1):
counter_DW01_inc_0/U2/b
-----------------------------------------
Net Name: counter_DW01_inc_0/SUM|7
Connections (1):
counter_DW01_inc_0/U2/x
-----------------------------------------
Net Name: counter/internal|7
Connections (3):
counter/add_13/SUM|7
counter_DW01_inc_0/SUM|7
counter/\count_reg[7]/d
-----------------------------------------
Net Name: counter/count|7
Connections (3):
counter/add_13/A|7
counter_DW01_inc_0/A|7
counter/\count_reg[7]/q
-----------------------------------------
Net Name: counter_DW01_inc_0/carry|7
Connections (2):
counter_DW01_inc_0/U1_1_6/co
counter_DW01_inc_0/U2/a
```

Gatepin is also a Net

Net gatepins

- Tracing Gatepin `counter/count_reg[7]/q` connections?
  - Net connection ➔ `count[7]`
- Tracing Gatepin `counter/count_reg[7]/d` connections?
  - Net connection ➔ `internal[7]`

Net-based Connectivity



Nets:

```
Net Name: counter_DW01_inc_0/A|7
Connections (1):
counter_DW01_inc_0/U2/b
-----------------------------------------
Net Name: counter_DW01_inc_0/SUM|7
Connections (1):
counter_DW01_inc_0/U2/x
-----------------------------------------
Net Name: counter/internal|7
Connections (3):
counter/add_13/SUM|7
counter_DW01_inc_0/SUM|7
counter/\count_reg[7]/d
-----------------------------------------
Net Name: counter/count|7
Connections (3):
counter/add_13/A|7
counter_DW01_inc_0/A|7
counter/\count_reg[7]/q
-----------------------------------------
Net Name: counter_DW01_inc_0/carry|7
Connections (2):
counter_DW01_inc_0/U1_1_6/co
counter_DW01_inc_0/U2/a
```

Net gatepins

Net is also gatepin

- Tracing Gatepin `counter_DW01_inc_0/U2/x` connections?
  - Net connection ➔ `counter_DW01_inc_0/SUM|7`
  - Net is also a gatepin, must be added and its net traced