

ASP Timer

STA Engine Technical Report

Propagate Delay Longest Path BFS Example

current

successors

Data1

Data2

CLK

Data3

DFP1

DFP2

NAND1

NAND2

BUF

DFP3

Out1

Out2

2

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Propagate Delay Longest Path BFS Example

current

successors

▶ 3

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10/11/2024

3

Propagate Delay Longest Path BFS Example

current

successors

Data 1

▶ 4

ASP Timer

10/11/2024

4

Propagate Delay Longest Path BFS Example

current

successors

Data I

5

ASP Timer

10/11/2024

5

Propagate Delay Longest Path BFS Example

current

successors

Data I

6

ASP Timer

10/11/2024

6

Propagate Delay Longest Path BFS Example

current

successors

Data1

Data2

The circuit diagram shows four inputs: Data1, Data2, CLK, and Data3. Data1 and Data2 are connected to two DFFs (DFF1 and DFF2). The outputs of DFF1 and DFF2 are connected to the inputs of NAND1. The output of NAND1 is connected to the input of NAND2. The output of NAND2 is connected to the input of a BUF (buffer). The output of the BUF is connected to the input of DFF3. The output of DFF3 is connected to Out1. Data3 is connected to Out2. The circuit is at step 7 of a BFS propagation delay calculation.

7

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7

Propagate Delay Longest Path BFS Example

current

successors

Data1

Data2

The circuit diagram is identical to the one in slide 7, but with a red circle on the CLK input, indicating it is the current node in the BFS propagation delay calculation.

8

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8

Propagate Delay Longest Path BFS Example

current

successors

Data 1

Data 2

clock ports
isconstrained
field is set to
-1, so skip

9

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9

Propagate Delay Longest Path BFS Example

current

successors

Data 1

Data 2

10

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10

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2

11ASP Timer10/11/2024

11

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3

12ASP Timer10/11/2024

12

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3

13

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13

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3

14

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14

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q

15

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15

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q

16

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16

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q

17

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10/11/2024

17

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q

18

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10/11/2024

18

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q

19

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10/11/2024

19

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q

20

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10/11/2024

20

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q
	DFF2/Q

21

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21

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q
	DFF2/Q

22

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22

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q
	DFF2/Q

23

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23

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q
	DFF2/Q

24

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10/11/2024

24

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q
	DFF2/Q

25

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10/11/2024

25

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q
	DFF2/Q

26

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26

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q
	DFF2/Q
	DFF3/Q

27

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27

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q
	DFF2/Q
	DFF3/Q

28

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28

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q
	DFF2/Q
	DFF3/Q

29 ASP Timer 10/11/2024

29

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q
	DFF2/Q
	DFF3/Q

30 ASP Timer 10/11/2024

30

Propagate Delay Longest Path BFS Example

current	successors
	Data1
	Data2
	Data3
	DFF1/Q
	DFF2/Q
	DFF3/Q

replace

31 ASP Timer 10/11/2024

31

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

Swapping is equivalent to level increment.

32 ASP Timer 10/11/2024

32

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

If the PI has been constrained by an SDC command then we propagate the cell_rise, cell_fall, rise_transition and fall_transition times to the FF's input.

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33

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

If the incoming path is been constrained and the FF pins' isconstrained field is set to 1 (FF is clocked) then we keep the isconstrained field to 1. Else set to zero (to be easily identified as unconstrained by the RAT propagation algorithm)

34 ASP Timer 10/11/2024

34

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

FF input gatepin is STA endpoint, so prevent adding component's outputs on successors

35 ASP Timer 10/11/2024

35

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

36 ASP Timer 10/11/2024

36

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

37 ASP Timer 10/11/2024

37

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

38 ASP Timer 10/11/2024

38

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

39ASP Timer10/11/2024

39

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

40ASP Timer10/11/2024

40

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

41

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41

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

42

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42

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

Mark the previous connections flag on input gatepins with 1 to prevent counting the inputs every time you reach the component. That way we count the input gatepins only 1 time.

Input gatepin's previous connections: 1

43 ASP Timer 10/11/2024

43

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

Component input gatepins count: 2

44 ASP Timer 10/11/2024

44

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

Mark the previous connections flag on input gatepins with 1 to prevent counting the inputs every time you reach the component. That way we count the input gatepins only 1 time.

Input gatepin's previous connections: 1

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45

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

Component input gatepins count: 3

46 ASP Timer 10/11/2024

46

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

Mark the previous connections
flag on input gatepins with 1
to prevent counting the inputs every
time you reach the component.
That way we count the input
gatepins only 1 time.

Input gatepin's
previous
connections: 1

47ASP Timer10/11/2024

47

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

Prev inputs = 3
Prev visited inputs = 1

48ASP Timer10/11/2024

48

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

49ASP Timer10/11/2024

49

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

50ASP Timer10/11/2024

50

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

51

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10/11/2024

51

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

52

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10/11/2024

52

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

53

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10/11/2024

53

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

54

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10/11/2024

54

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

55

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10/11/2024

55

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

56

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10/11/2024

56

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

57

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10/11/2024

57

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

58

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10/11/2024

58

Propagate Delay Longest Path BFS Example

current	successors
Data1	
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

Prev inputs = 3
Prev visited inputs = 3

59 ASP Timer 10/11/2024

59

Propagate Delay Longest Path BFS Example

current	successors
Data1	NAND1/ZN
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

Insert to successors

60 ASP Timer 10/11/2024

60

Propagate Delay Longest Path BFS Example

current	successors
Data1	NAND1/ZN
Data2	
Data3	
DFF1/Q	
DFF2/Q	
DFF3/Q	

Gatepin Out1 is not a component gatepin so it is not inserted in successors

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61

Propagate Delay Longest Path BFS Example

current	successors
Data1	NAND1/ZN
Data2	
DFF1/Q	
DFF2/Q	
DFF3/Q	

Reached last current output so free current array and replace it with successors

replace

62 ASP Timer 10/11/2024

62

Propagate Delay Longest Path BFS Example

current

successors

NAND1/ZN

Replace is equivalent to level increment.

63ASP Timer10/11/2024

63

Propagate Delay Longest Path BFS Example

current

successors

NAND1/ZN

Mark input as visited

64ASP Timer10/11/2024

64

Propagate Delay Longest Path BFS Example

current	successors
NAND1/ZN	

65 ASP Timer 10/11/2024

65

Propagate Delay Longest Path BFS Example

current	successors
NAND1/ZN	NAND2/ZN

66 ASP Timer 10/11/2024

66

Propagate Delay Longest Path BFS Example

current	successors
NAND1/ZN	NAND2/ZN

Reached last current output so free current array and replace it with successors

replace

▶ 67

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10/11/2024

67

Propagate Delay Longest Path BFS Example

current	successors
NAND2/ZN	

Replace is equivalent to level increment.

▶ 68

ASP Timer

10/11/2024

68

Propagate Delay Longest Path BFS Example

current	successors
NAND2/ZN	

69

ASP Timer

10/11/2024

69

Propagate Delay Longest Path BFS Example

current	successors
NAND2/ZN	

70

ASP Timer

10/11/2024

70

Propagate Delay Longest Path BFS Example

current	successors
NAND2/ZN	BUF/Z

71

ASP Timer

10/11/2024

71

Propagate Delay Longest Path BFS Example

current	successors
NAND2/ZN	BUF/Z

Reached last current output so free current array and replace it with successors

replace

72

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10/11/2024

72

Propagate Delay Longest Path BFS Example

current

successors

BUF/Z

Replace is equivalent to level increment.

73

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10/11/2024

73

Propagate Delay Longest Path BFS Example

current

successors

BUF/Z

FF input gatepin is STA endpoint, so prevent adding component's outputs on successors

74

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10/11/2024

74

Propagate Delay Longest Path BFS Example

current

successors

BUF/Z

Reached last current output
so free current array and
replace it with successors

replace

75

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10/11/2024

75

Propagate Delay Longest Path BFS Example

current

successors

Replace is equivalent to level
increment.

76

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10/11/2024

76

Propagate Delay Longest Path BFS Example

current

successors

Current array is empty after replace. Delay propagation algorithm has finished.

77ASP Timer10/11/2024

77

Propagate RAT Longest Path BFS Example

predecessors

current

78ASP Timer10/11/2024

78

Propagate RAT Longest Path BFS Example

predecessors

current

PO's unconstrained field was not set to 1 by an SDC command, so skip

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79

Propagate RAT Longest Path BFS Example

predecessors

current

FF's input unconstrained field has been set to 0 by delay propagation algorithm because the incoming path is not constrained, so skip.

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80

Propagate RAT Longest Path BFS Example

predecessors	current

FF's input isconstrained field has been set to 0 by delay propagation algorithm because the incoming path is not constrained, so skip.

81 ASP Timer 10/11/2024

81

Propagate RAT Longest Path BFS Example

predecessors	current
DFF3/D	

FF's input isconstrained field has been set to 1 by delay propagation algorithm because the incoming path is constrained and the FF is constrained too, so insert to predecessors.

82 ASP Timer 10/11/2024

82

Propagate RAT Longest Path BFS Example

predecessors	current
DFF3/D	

replace

83 ASP Timer 10/11/2024

83

Propagate RAT Longest Path BFS Example

predecessors	current
DFF3/D	

Replace is equivalent to level increment on the Transpose Graph.

84 ASP Timer 10/11/2024

84

Propagate RAT Longest Path BFS Example

predecessors	current
	DDF3/D

Fanout connections number has been stored by delay propagation algorithm. It also sets visited connections count to 0.

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85

Propagate RAT Longest Path BFS Example

predecessors	current
	DDF3/D

Every time we visit an output we increment the visited count. When visited equals fanout then we discover the predecessor inputs.

86 ASP Timer 10/11/2024

86

Propagate RAT Longest Path BFS Example

predecessors	current
	DFF3/D

87

ASP Timer

10/11/2024

87

Propagate RAT Longest Path BFS Example

predecessors	current
	DFF3/D

88

ASP Timer

10/11/2024

88

Propagate RAT Longest Path BFS Example

predecessors	current
BUF/I	DF3/D

Insert to predecessors.

89 ASP Timer 10/11/2024

89

Propagate RAT Longest Path BFS Example

predecessors	current
BUF/I	DF3/D

Reached last current input so free current array and replace it with predecessors

replace

90 ASP Timer 10/11/2024

90

Propagate RAT Longest Path BFS Example

predecessors

current

BUF/I

Replace is equivalent to level increment on the Transpose Graph.

91

ASP Timer

10/11/2024

91

Propagate RAT Longest Path BFS Example

predecessors

current

BUF/I

Fanout connections number has been stored by delay propagation algorithm. It also sets visited connections count to 0.

92

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10/11/2024

92

predecessors

current

BUF/I

93

ASP Timer

10/11/2024

Propagate RAT Longest Path BFS Example

Every time we visit an output we increment the visited count. When visited equals fanout then we discover the predecessor inputs.

The circuit diagram shows a sequence of components: Data1 and Data2 are inputs to DFF1 and DFF2. Data3 is an input to NAND1. CLK is a common clock signal. The output of DFF1 goes to NAND1. The output of DFF2 goes to NAND1. The output of NAND1 goes to NAND2. The output of NAND2 goes to BUF. The output of BUF goes to DFF3. The output of DFF3 goes to Out1. Out2 is also an output of the circuit. A red line highlights the path from Data2 through NAND1, NAND2, and BUF to Out1. A callout bubble explains the visited count logic.

93

predecessors

current

BUF/I

94

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10/11/2024

Propagate RAT Longest Path BFS Example

Note that gatepin NAND2/ZN fanouts to Primary Output Out2, too, but we consider only component gatepins on the BFS counts.

The circuit diagram is identical to slide 93. A red line highlights the path from Data2 through NAND1, NAND2, and BUF to Out1. A red 'X' marks the fanout from NAND2/ZN to Out2. A callout bubble explains that only component gatepins are considered for BFS counts.

94

Propagate RAT Longest Path BFS Example

predecessors	current
	BUF/I

Identically with delay propagation algorithm we count the previous gatepins to add an input to predecessors only if every output gatepin of the same component has been visited.

Prev outputs count: 1
Prev visited outputs count : 1

95 ASP Timer 10/11/2024

95

Propagate RAT Longest Path BFS Example

predecessors	current
NAND2/A	BUF/I

Insert to predecessors.

96 ASP Timer 10/11/2024

96

Propagate RAT Longest Path BFS Example

predecessors	current
NAND2/A	BUF/I

97ASP Timer10/11/2024

97

Propagate RAT Longest Path BFS Example

predecessors	current
NAND2/A	BUF/I

98ASP Timer10/11/2024

98

Propagate RAT Longest Path BFS Example

predecessors

current

NAND2/A

Replace is equivalent to level increment on the Transpose Graph.

99ASP Timer10/11/2024

99

Propagate RAT Longest Path BFS Example

predecessors

current

NAND2/A

Fanout connections number has been stored by delay propagation algorithm. It also sets visited connections count to 0.

100ASP Timer10/11/2024

100

Propagate RAT Longest Path BFS Example

predecessors

current

NAND2/A

Every time we visit an output we increment the visited count. When visited equals fanout then we discover the predecessor inputs.

101ASP Timer10/11/2024

101

Propagate RAT Longest Path BFS Example

predecessors

current

NAND2/A

Identically with delay propagation algorithm we count the previous gatepins to add an input to predecessors only if every output gatepin of the same component has been visited.

Prev outputs count: 1
Prev visited outputs count : 1

102ASP Timer10/11/2024

102

Propagate RAT Longest Path BFS Example

predecessors	current
NAND1/A	NAND2/A

103

ASP Timer

10/11/2024

103

Propagate RAT Longest Path BFS Example

predecessors	current
NAND1/A	NAND2/A

Identically with delay propagation algorithm we count the previous gatepins to add an input to predecessors only if every output gatepin of the same component has been visited.

Prev outputs count: 1
Prev visited outputs count : 1

104

Propagate RAT Longest Path BFS Example

predecessors	current
NAND1/A	NAND2/A
NAND1/B	

105

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10/11/2024

105

Propagate RAT Longest Path BFS Example

predecessors	current
NAND1/A	NAND2/A
NAND1/B	

106

ASP Timer

10/11/2024

106

Propagate RAT Longest Path BFS Example

predecessors	current
NAND1/A	NAND2/A
NAND1/B	

Reached last current input
so free current array and
replace it with predecessors

replace

107 ASP Timer 10/11/2024

107

Propagate RAT Longest Path BFS Example

predecessors	current
	NAND1/A
	NAND1/B

Reached FF output. RAT
propagation endpoint.

108 ASP Timer 10/11/2024

108

Propagate RAT Longest Path BFS Example

predecessors	current
	NAND1/A
	NAND1/B

Reached FF output. RAT propagation endpoint.

109 ASP Timer 10/11/2024

109

Propagate RAT Longest Path BFS Example

predecessors	current
	NAND1/A
	NAND1/B

Reached last current input so free current array and replace it with predecessors

replace

110 ASP Timer 10/11/2024

110

Propagate RAT Longest Path BFS Example

predecessors

current

Current array is empty after replace. RAT propagation algorithm has finished.

111 ASP Timer 10/11/2024

111

Back-trace Longest Path Example

Assume gatepin DFF3/D has been found as the minimum slack path endpoint.

112 ASP Timer 10/11/2024

112

Back-trace Longest Path Example

113ASP Timer10/11/2024

113

Back-trace Longest Path Example

114ASP Timer10/11/2024

114

Back-trace Longest Path Example

115ASP Timer10/11/2024

115

Back-trace Longest Path Example

116ASP Timer10/11/2024

116

Back-trace Longest Path Example

117ASP Timer10/11/2024

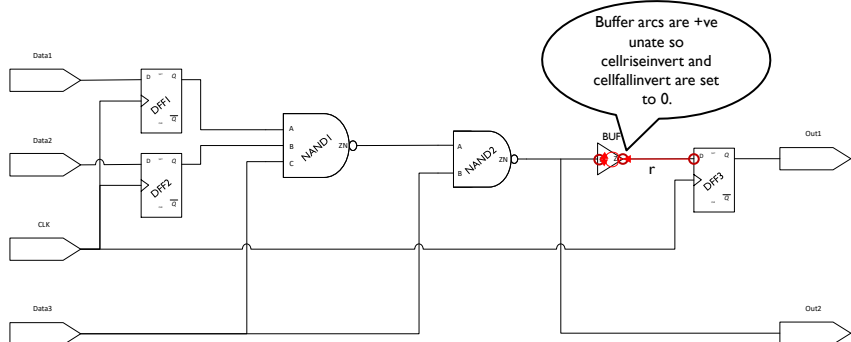
117

Back-trace Longest Path Example

118ASP Timer10/11/2024

118

Back-trace Longest Path Example



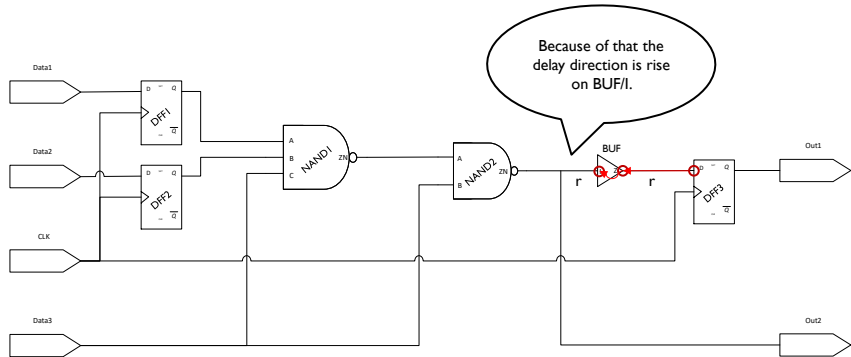
119

ASP Timer

10/11/2024

119

Back-trace Longest Path Example



120

ASP Timer

10/11/2024

120

Back-trace Longest Path Example

121

ASP Timer

10/11/2024

121

Back-trace Longest Path Example

122

ASP Timer

10/11/2024

122

Back-trace Longest Path Example

NAND gate's arcs are -ve unate so both cellriseinvert and cellfallinvert fields are set to 1.

123ASP Timer10/11/2024

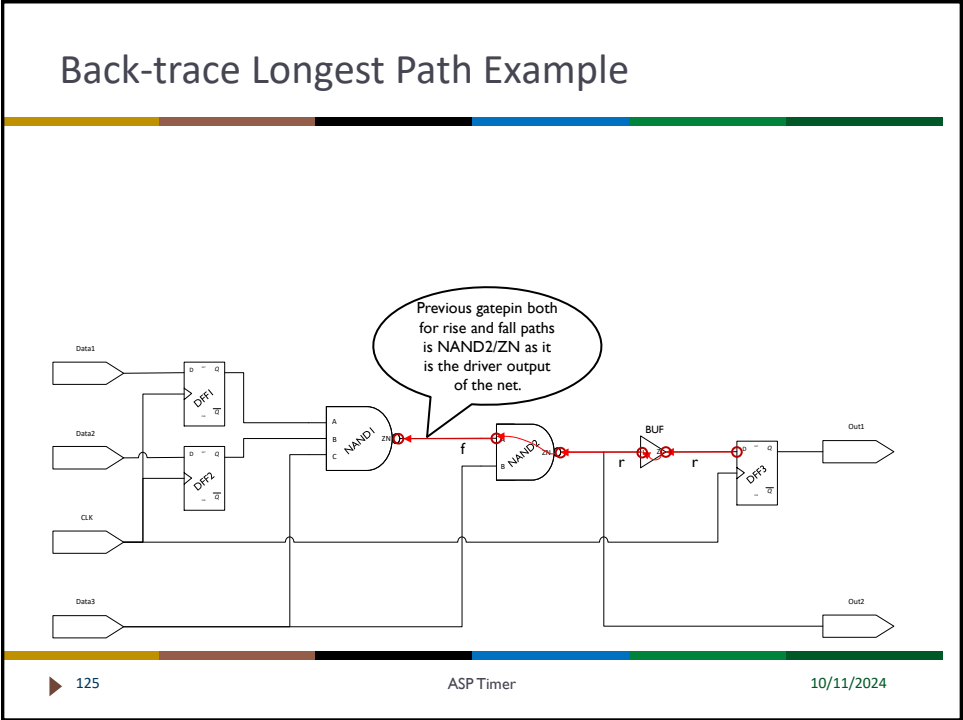
123

Back-trace Longest Path Example

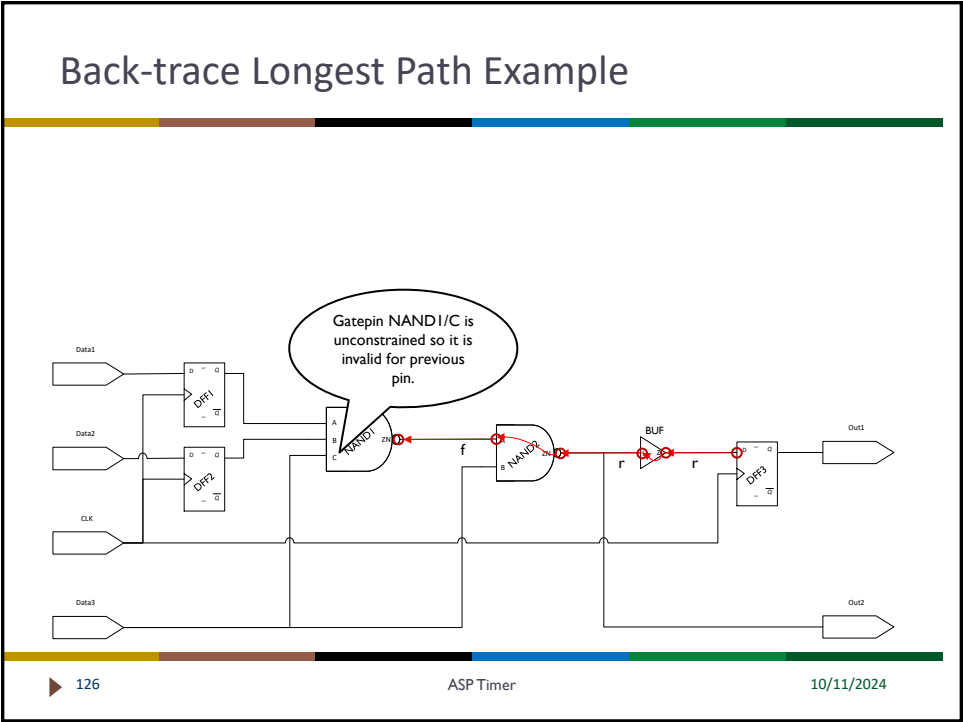
Because of that the delay direction is fall on NAND2/A.

124ASP Timer10/11/2024

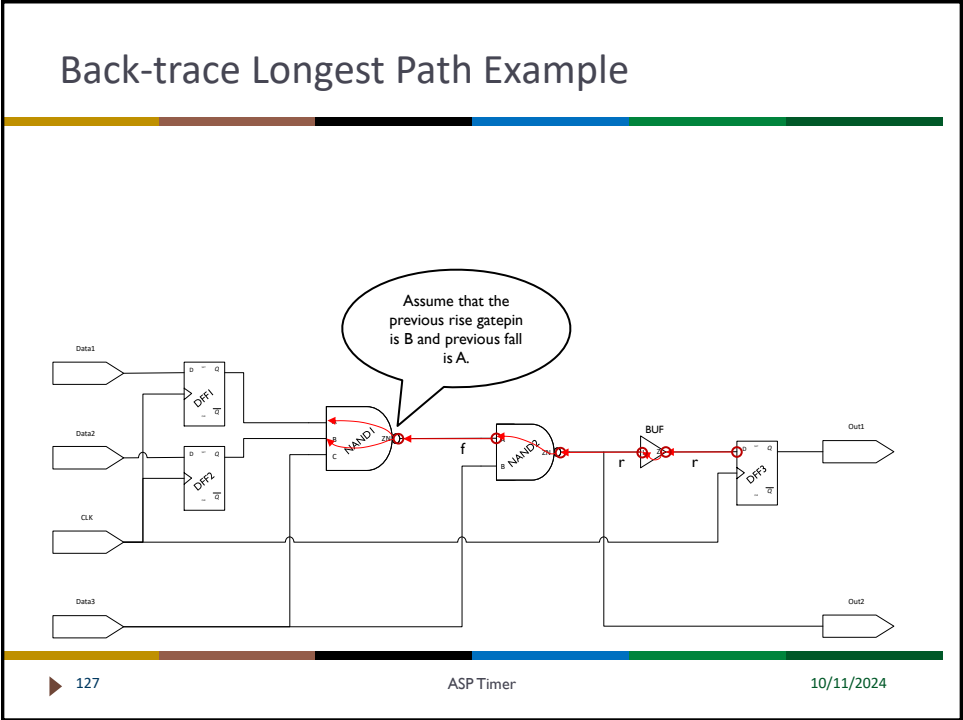
124



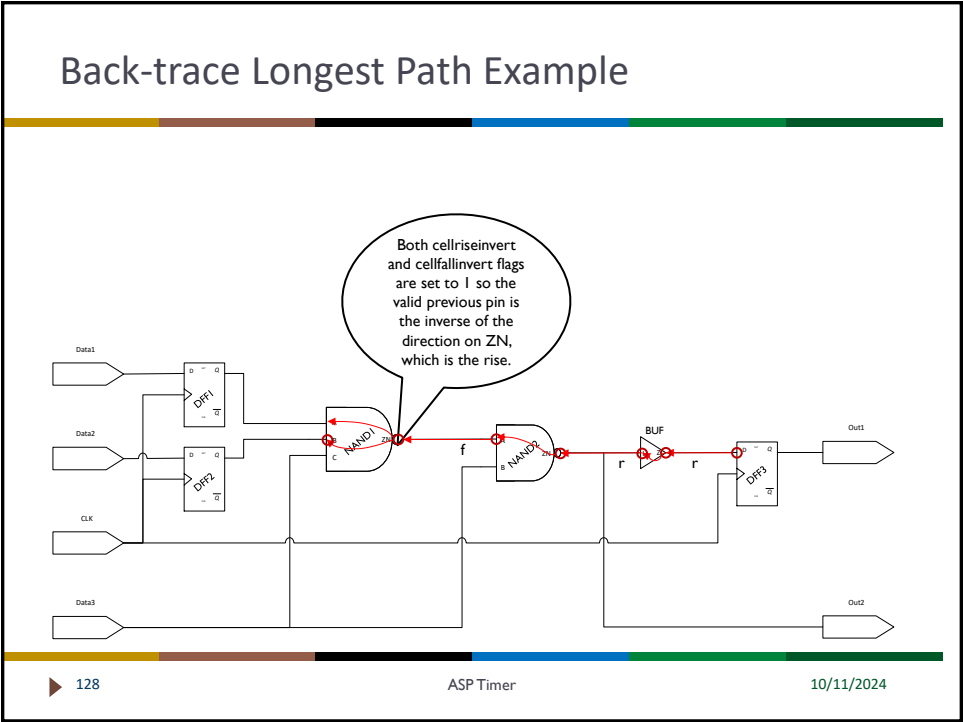
125



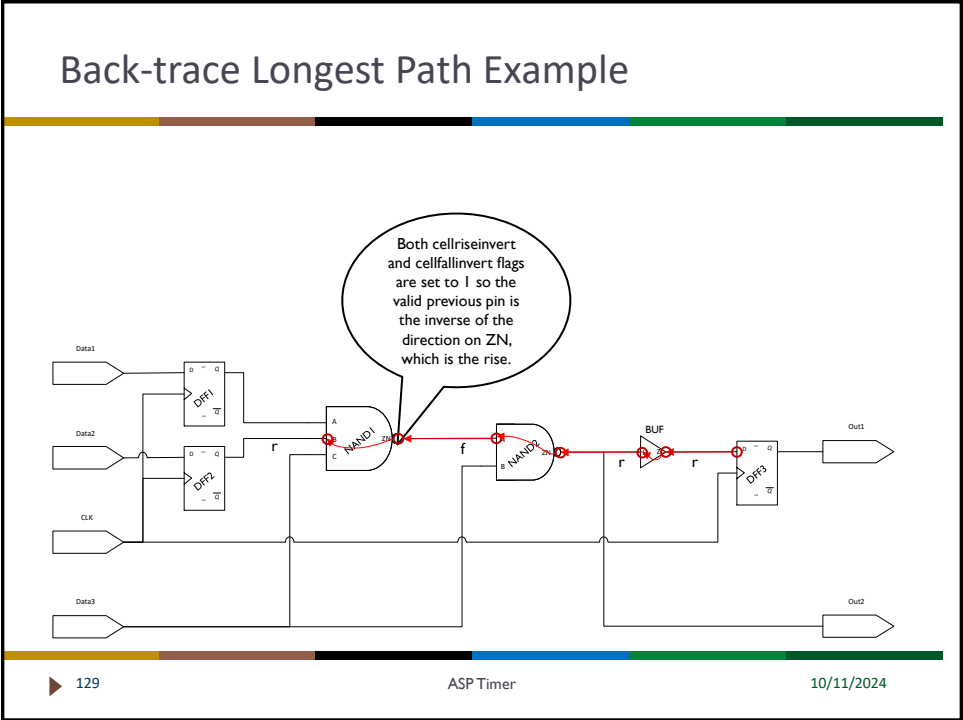
126



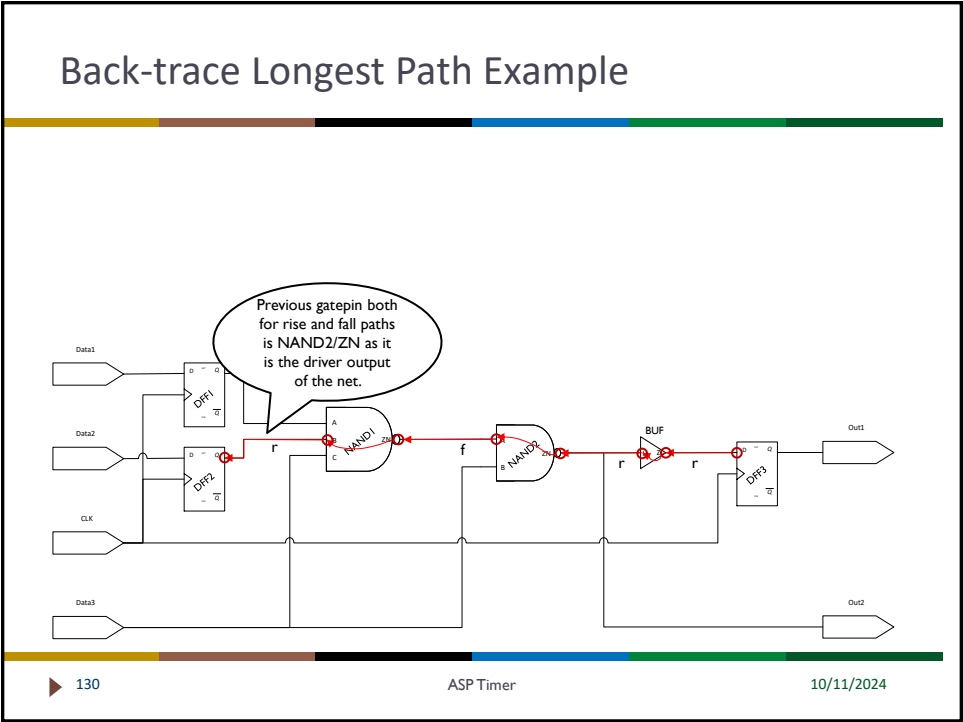
127



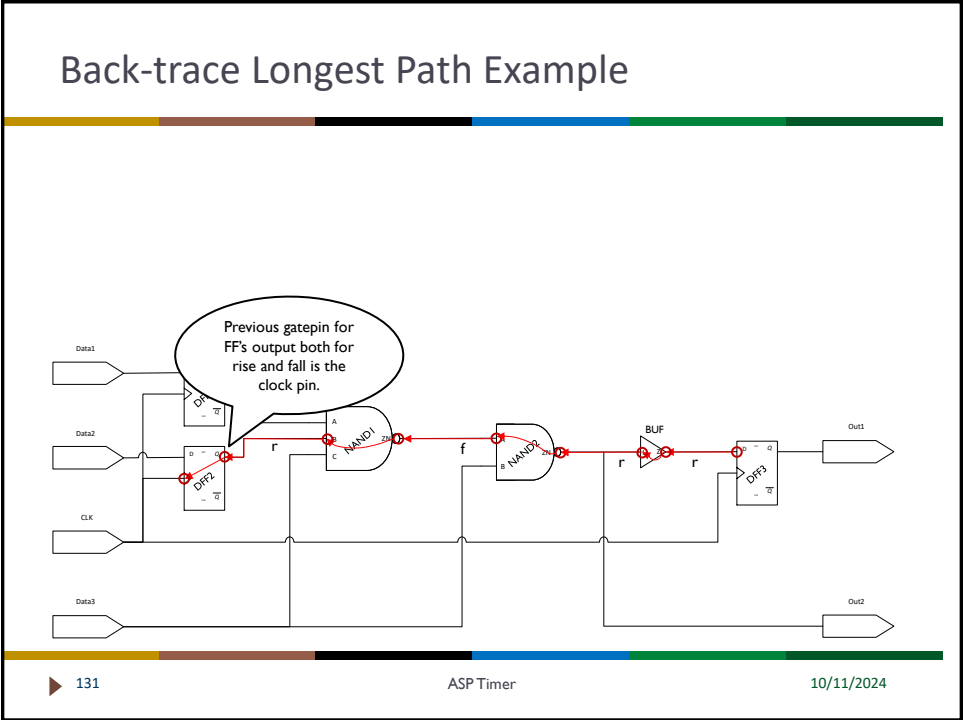
128



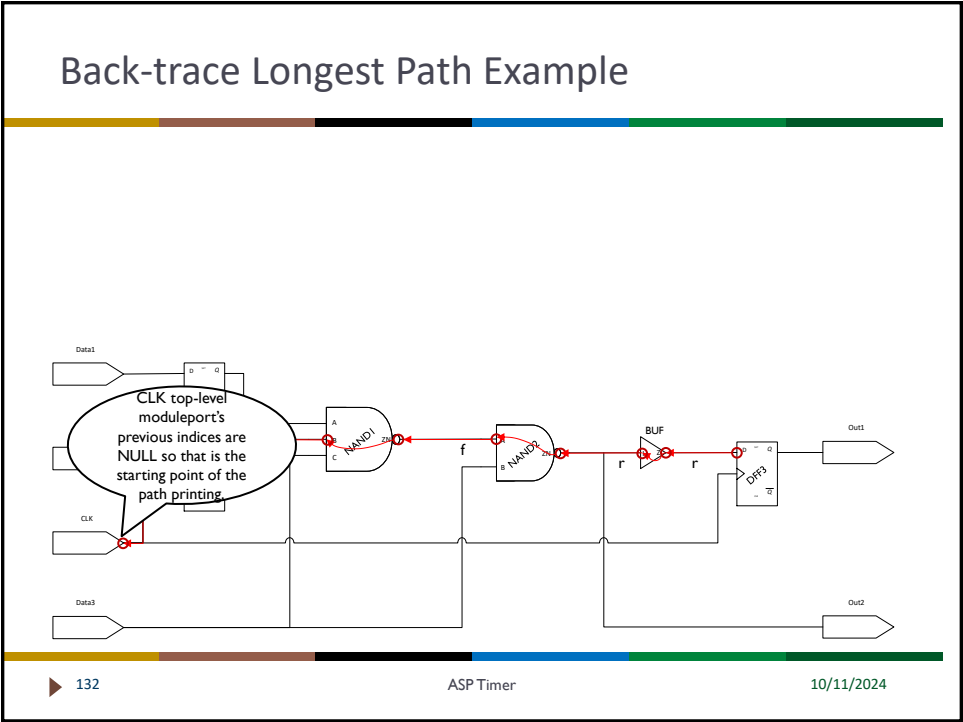
129



130

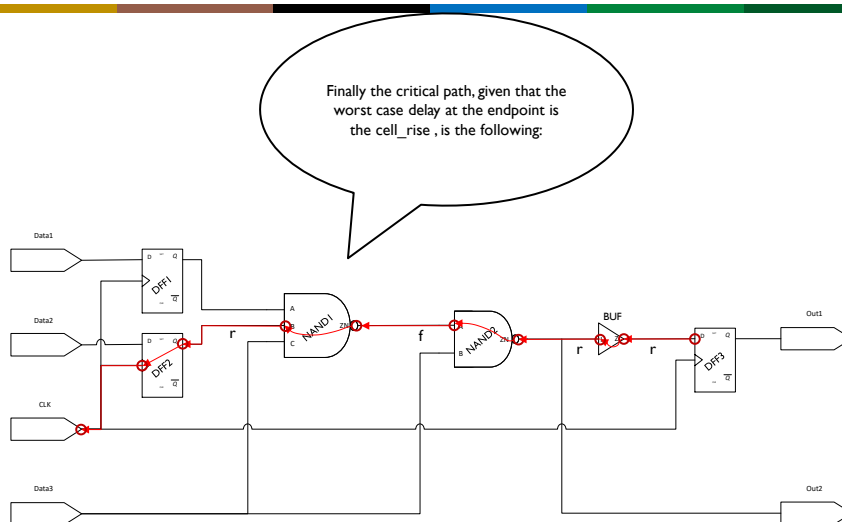


131



132

Back-trace Longest Path Example



▶ 133

ASP Timer

10/11/2024

133

Shortest Path Analysis

- ▶ The above practices can be applied for best case analysis too.
- ▶ The difference is that we get instead of max delay and transition values, the min ones.
- ▶ Also, in terms of levelisation we store the level in the first occurrence of a gatepin instead of the last one (classic BFS).
- ▶ In RAT propagation we keep the max value instead of min.
- ▶ RAT on endpoints is the hold time of the Flip-Flop. (Contrary to longest path RAT which is clock period – setup time)

▶ 134

ASP Timer

10/11/2024

134

References

- ▶ Timing Arcs and Unateness:
 - ▶ <http://www.vlsi-expert.com>
 - ▶ <http://vlsiuniverse.blogspot.com>
- ▶ Simulation
 - ▶ <https://www.swarthmore.edu/NatSci/echeeve I/Ref/mna/MNA2.html>