









































<pre>module TOK_BUF(L, R); parameter width = 8; parameter init = 8'b0; 'INPORT(L,width); 'OUTPORT(R,width); 'USES_CHANNEL parameter FL = 2; parameter BL = 4; reg [width-1:0] d; initial begin `SEND(R,init); end always begin `RECEIVE(L,d); #FL; `SEND(R,d); #BL; end endmodule</pre> <pre> Initial block Mechanism to send out initial token Mechanism to send out token Mechanism Mechanism</pre>	Token Buffer – VerilogCSP Model	
	<pre>parameter width = 8; parameter init = 8'b0; `INPORT(L,width); `OUTPORT(R,width); `USES_CHANNEL parameter FL = 2; parameter BL = 4; reg [width-1:0] d; initial begin `SEND(R,init); end always begin `RECEIVE(L,d); #FL; `SEND(R,d); #BL; end</pre>	 Mechanism to send out initial token Init Value of initial token sent out Configurable via Verilog parameter feature After initial block, never used again Always block Performs steady-state behavior















