University of Thessaly - Electrical and Computer Engineering Department

CE664- Asynchronous Circuit Design

Spring Term - Academic Year 2015-2016

2nd Assignment

5/11/2015 to 21/11/2015

C. P. Sotiriou

2nd Assignment's Goal

Each assignment is composed of one or more task, which require thought, design, programming or a combination of all. The goal of the 2nd assignment is to familiarise you with the use of asynchronous handshaking templates, and their interconnection into useful practical circuits.

Task 1 (Implement Merge, Split, Special Split, Arbiter and Copy Templates)

Implement the 5 basic, **4-phase**, handshake channel templates reviewed in the course handouts using C-elements or Verilog standard gate primitives, *i.e.* the 2-element merge, with DR select signal, the 2-element split, the special-split, which converts a 1-bit bundled data into a DR signal with acknowledgement, the arbiter (without a metastability filter - behaviourally only) and the copy cell.

The delay of gates should be parameterised and specified as follows: C-elements - 1ns, OR/AND gates - 0.5ns, MUX - 0.7ns, XOR/XNOR gates - 0.9ns. For each template, provide (i) block diagram illustrating the handshake signals and data ports, (ii) PTnet specification, (iii) implementation schematic with annotated delays and the bundled-data margin calculated and (iv) simulation waveforms.

Task 2 (Implement 2x2 Asynchronous Crossbar Template)

By using the templates of Task 1, implement the 2x2 Asynchronous Crossbar template found in the lecture notes, and measure its latency and throughput for each point to point link. Present simulation results for your measurements. Are you able to relate the latency to the delays of the templates?

Task 3 (Implement 4x4 Crossbar using 2x2 Crossbar Templates)

Now, using the 2x2 Crossbar and 2-bit addresses implement a 4x4 Crossbar. Again measure the 4x4 Crossbar's latency and throughput for each point to point link, and present simulation results which justify your measurements.

Deadline and Submission

The deadline for the 1st Assignment Set is **31/3/2014**. You should submit your solution set, before the dealine, via the `e-Class` portal.