University of Thessaly - Electrical and Computer Engineering Department

CE664 - Asynchronous Circuit Design

Spring Term - Academic Year 2015-2016

1st Assignment

16/10/2015 to 2/11/2015

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1st Assignment's Goal

Each assignment is composed of one or more task, which require thought, design, programming or a combination of all. The goal of the 1st assignment is to familiarise you with the simplest type of asynchronous pipelines, *i.e.* micropipeline and mousetrap-based control, coupled with bundled-data datapath, and its basic circuit and performance characteristics.

Task 1 (C Element Specification and Verilog Simulation)

(a) Implement two-input,**resettable** C elements (one resetting to 0, another to 1) in **behavioural Verilog** (non synthesisable). The C element's Verilog specification should include, as a parameter, the C element's delay, and generate output events (on output `c`) as a response to input events (inputs `a` and `b`). By setting the C element delay to 1ns, for a hypothetical process, verify correct operation via Simulation and present relevant waveforms and/or simulation output. Similarly, create an XOR gate, with a parameterised delay, and set its default value to 800ps.

Task 2 (Micropipeline, Mousetrap Pipeline Verilog Simulation)

(a) Using the 1ns C element from Task 1, implement a linear micropipeline of 3 stages, and simulate its behaviour for: (i) fast transmitter, slow receiver, (ii) slow transmitter, fast receiver, (iii) fast transmitter, fast receiver. Illustrate simulation waveforms and relevant output which indicates correct operation (think about what correct operation means...).

(b) Attach a 3-stage, 4-phase, **4-bit bundled-data datapath**, *i.e.* three 4-bit Data Latches per pipeline stage, to the micropipeline and mousetrap control of Task 2(a). For a data sequence of data tokens A, B, C, D illustrate their transmission/reception, from the LHS Sender H/S to the RHS Receiver H/S, with appropriate simulation waveforms. Determine, via simulation, the Latency, Data Token Cycle Time (Delay between Tokens) and Throughput (Data Tokens/Sec) of your two pipelines. Reason about how these metrics depend on the gate and/or wire delays of the implementation.

Task 3 (Micropipeline Ring in PIPE2)

(a) Build a 3 stage micropipeline ring's PTnet in PIPE2, by connecting together the three PTnets of each stage, as well as the `Rout = Rin`, `Ain = Aout` arcs. Verify, using State Space Analysis, and **illustrating your initial marking**, that the ring deadlocks if **all C elements reset to 0**. Illustrate the State Reachability Graph and briefly explain it.

(b) Based on the MSFSMs (Multiple Synchronised FSMs) model of the 3 stage ring, identify an MSFSM initial marking (set of initial states of the FSMs, and initial environment states) which **renders the system live**. Then, assign this marking onto the PTnet of (a) and verify liveness using State Space Analysis. Illustrate, in this case, the State Reachability Graph and briefly explain it.

Deadline and Submission

The deadline for the 1st Assignment Set is **2/11/2015**. You should submit your solution set, before the dealine, via the `e-Class` portal.