ECE658– Advanced Topics in Computer Architecture

Homework 1

Due on Tuesday, November 6, 2018

ASSIGNMENTS SHOULD BE TURNED IN **INDIVIDUALLY**

1. **Basic cache functionality.** Assume that the following memory addresses are generated by the CPU due to the execution of load or store instructions:

   4, 16, 248, 80, 20, 76, 208, 36, 172, 44 (all are byte addresses in decimal radix)

   These addresses are presented to a 64 byte L1 Data Cache which is initially empty. This exercises asks that you draw the contents of the Data Cache after each access (data array, tag, valid bits), assuming a 2-way set associative cache, with 8 bytes block size, using Least Recently Used (LRU) algorithm to decide which block to evict. The main memory is 512 bytes in size.

2. **Branch prediction.** Suppose we have a deeply pipelined processor, for which we implement a branch target buffer (BTB) for the conditional branches only. Assume that the misprediction penalty is always 5 cycles and the buffer miss penalty is always 2 cycles. Assume 90% hit rate and 90% accuracy (in case of a BTB hit), and 15% branch frequency. How much faster is the processor with the branch target buffer versus a processor that has a fixed 2-cycle branch penalty? Assume a base CPI without branch stalls of 1. Note: study example of page 123 in H&P, v. 4 before you attempt this problem.

3. **Cache performance optimization.** Exercises 5.6, 5.7 of H&P, version 4. Assume that a double precision array element is 8 bytes. Assume that each array occupies 8 KB of the cache. Note: Study examples at page 307 and 308 before you attempt this exercise.