University of Thessaly - Electrical and Computer Engineering Department

# CE653 - Asynchronous Circuit Design

Spring Term - Academic Year 2020-2021

**1st Assignment**

*3/3/2021 to 18/3/2021*

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## 1st Assignment's Goal

Each assignment is composed of one or more task, which require thought, design, programming or a combination of all. The goal of the 1st assignment is to familiarise you with the simplest type of asynchronous pipeline, *i.e.* micropipeline control coupled with bundled-data datapath, and its basic circuit and performance characteristics.

## Task 1 (C Element Specification and Verilog Simulation)

(a) Implement two-input,*resettable* C elements (one resetting to 0, another to 1) in behavioural Verilog (non synthesisable). The C element's Verilog specification should include, as a parameter, the C element's delay, and generate output events (on output `c`) as a response to input events (inputs `a` and `b`). Setting the C element delay to 1ns, verify correct operation via Simulation and present relevant waveforms and/or simulation output.

(b) Based on the combinational logic two-input, C element implementation (`c = ab + c(a + b)`), present a modified Boolean equation which includes an active-high reset signal.

## Task 2 (Micropipeline Verilog Simulation)

(a) Using the 1ns C element from Task 1, implement a linear micropipeline of 3 stages, and simulate its behaviour for: (i) fast transmitter, slow receiver, (ii) slow transmitter, fast receiver, (iii) fast transmitter, fast receiver. Illustrate simulation waveforms and relevant output which indicates correct operation (think about what correct operation means...).

(b) Attach four-phase bundled-data datapath to the micropipeline of Task 2(a). For a data sequence of data tokens A, B, C, D illustrate their correct transmission/reception with the appropriate simulation waveforms. Compute, via simulation, the total time required to push the four data tokens through the micropipeline. Illustrate that the computed result is correct, by showing the relation of the data token latency on a single micropipeline stage PTnet, and the impact of C gate delay on the PTnet.

# Task 3 (Micropipeline Ring in PIPE2)

(a) Build the 3 stage micropipeline ring's PTnet in PIPE2, by connecting together the three PTnets of each stage, as well as the `Rout = Rin`, `Ain = Aout` arcs. Verify, using State Space Analysis, and illustrating your initial marking, that the ring deadlocks if all C elements reset to 0. Illustrate the State Reachability Graph and briefly explain it.

(b) Based on the MSFSMs (Multiple Synchronised FSMs) model of the 3 stage ring, identify an initial marking (set of initial states of the FSMs, and initial environment states) which renders the system live. Then, assign this marking onto the PTnet of (a) and verify liveness using State Space Analysis. Illustrate, in this case, the State Reachability Graph and briefly explain it.

# Deadline and Submission

The deadline for the 1st Assignment Set is **18/3/2021**. You should submit your solution set, before the dealine, via the `e-Class` portal.