Static Probabilities Annotation

Christos P. Sotiriou

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Static Probabilities

- The static probabilities provide a general insight into the circuit's state, indicating the probability of a gate pin being at a specific logic state, i.e. logic-1 or logic-0
  - $SP_1(G_i)$ indicates the probability of a gate pin G_i being at logic-1
    - $SP_1(G_i) = 1$ → gatepin G_i is always at logic-1 state
      - Accordingly, for $SP_1(G_i) = 0$
- Static probabilities are used in several steps of design
  - such as power and heat estimation

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Static Probabilities Annotation (0-Algorithm)

- The most common algorithm used by industrial tools is the one called 0-Algorithm by Parker and McCluskey [1]
- The following table presents the equations for the static probabilities for the most common logic gates

Logic Gate	Probability Equation
AND2	$P_1(out) = P_1(a) \times P_1(b)$
OR2	$P_1(out) = P_1(a) + P_0(a) \times P_1(b)$
NAND2	$P_1(out) = P_0(a) + P_1(a) \times P_0(b)$
NOR2	$P_1(out) = P_0(a) \times P_0(b)$
XOR2	$P_1(out) = \big(P_0(a) \times P_1(b)\big) + \big(P_1(a) \times P_0(b)\big)$
XNOR2	$P_1(out) = \big(P_0(a) \times P_0(b)\big) + \big(P_1(a) \times P_1(b)\big)$
INV	$P_1(out) = P_0(a)$
BUF	$P_1(out) = P_1(a)$

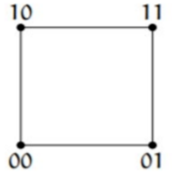
[1] K. P. Parker and E. J. McCluskey, “Probabilistic treatment of general combinational networks,” *IEEE Transactions on Computers*, vol. 100, no. 6, 1975.

Static Probabilities Annotation (0-Algorithm)

- How these equations are extracted?
- OR

a	b	F
0	0	0
0	1	1
1	0	1
1	1	1

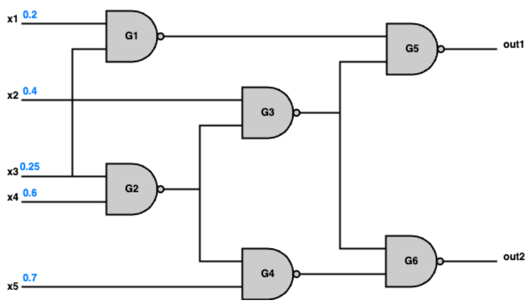
$$ONset = \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 1 & 1 \end{bmatrix} = \begin{bmatrix} 1 & - \\ 0 & 1 \end{bmatrix}$$



$$\rightarrow P_1(F) = P_1(a) + P_0(a) \times P_1(b)$$

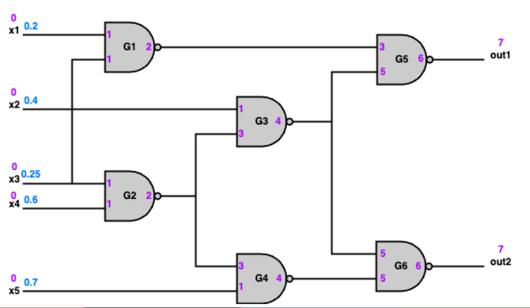
Example

- Let static probabilities for starting points
  - $P_1(x1) = 0.2$
  - $P_1(x2) = 0.4$
  - $P_1(x3) = 0.25$
  - $P_1(x4) = 0.6$
  - $P_1(x5) = 0.7$



Example

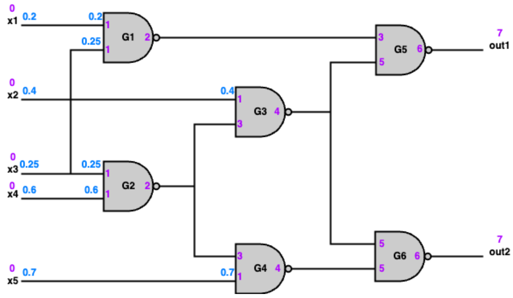
- The circuit graph must be levelised before the static probabilities annotation
  - the input pins of a gate must be already annotated before the annotation of the gate output pin
    - annotated with purple in the schematic



Example

- Level 1:
  - $P_1(G1|A) = P_1(x1) = 0.2$ $\quad$ $P_1(G1|B) = P_1(x3) = 0.25$
  - $P_1(G2|A) = P_1(x3) = 0.25$ $\quad$ $P_1(G2|B) = P_1(x4) = 0.6$
  - $P_1(G3|A) = P_1(x2) = 0.4$
  - $P_1(G4|B) = P_1(x5) = 0.7$

The static probabilities for an input pin of a gate is equal to the static probability of the net driver



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Example

- Level 2:
  - G1 → NAND2: $P_1(G1|Q) = P_0(G1|A) + P_1(G1|A) \times P_0(G1|B) = 0.95$
  - G2 → NAND2: $P_1(G2|Q) = P_0(G2|A) + P_1(G2|A) \times P_0(G2|B) = 0.85$
- Level 3:
  - $P_1(G5|A) = P_1(G1|Q) = 0.95$
  - $P_1(G3|B) = P_1(G2|Q) = 0.85$
  - $P_1(G4|A) = P_1(G2|Q) = 0.85$

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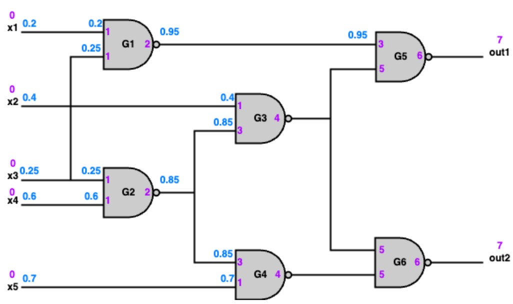

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Example

- Level 4:
  - G3 → NAND2: $P_1(G3|Q) = P_0(G3|A) + P_1(G3|A) \times P_0(G3|B) = 0.66$
  - G4 → NAND2: $P_1(G4|Q) = P_0(G4|A) + P_1(G4|A) \times P_0(G4|B) = 0.405$
- Level 5:
  - $P_1(G5|B) = P_1(G3|Q) = 0.66$
  - $P_1(G6|A) = P_1(G3|Q) = 0.66$
  - $P_1(G6|B) = P_1(G4|Q) = 0.405$

Logic Gate	Probability Equation
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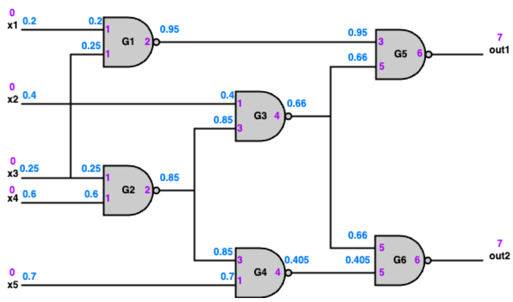

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Example

- Level 6:
  - G5 → NAND2: $P_1(G5|Q) = P_0(G5|A) + P_1(G5|A) \times P_0(G5|B) = 0.374$
  - G6 → NAND2: $P_1(G6|Q) = P_0(G6|A) + P_1(G6|A) \times P_0(G6|B) = 0.733$
- Level 7:
  - $P_1(out1) = P_1(G5|Q) = 0.374$
  - $P_1(out2) = P_1(G6|Q) = 0.733$

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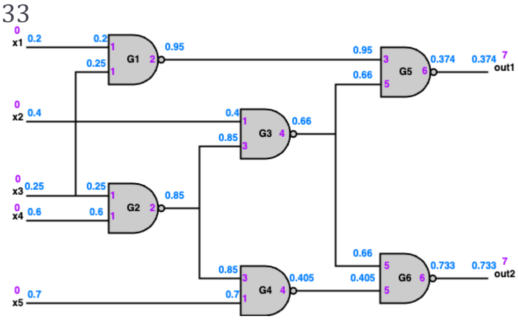

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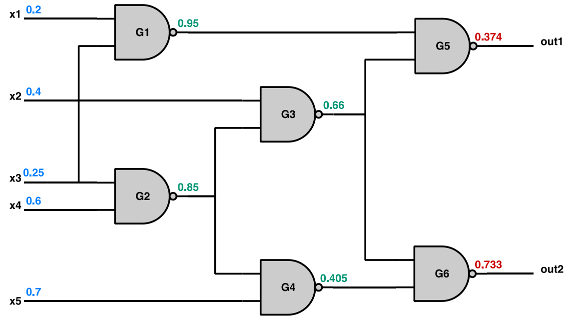
Reconvergence

- **(+) Fast probabilities annotation**
- **(-) Not so accurate**
- 0-Algorithm totally **IGNORES *signal correlations***
  - exist in circuit due to **reconvergent** paths



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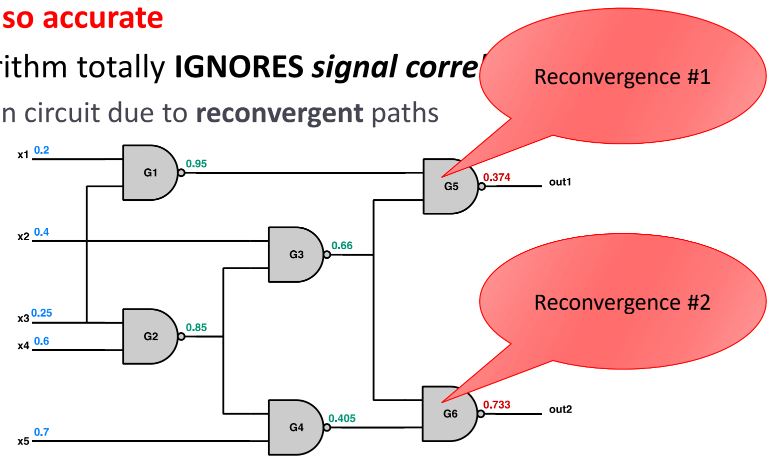

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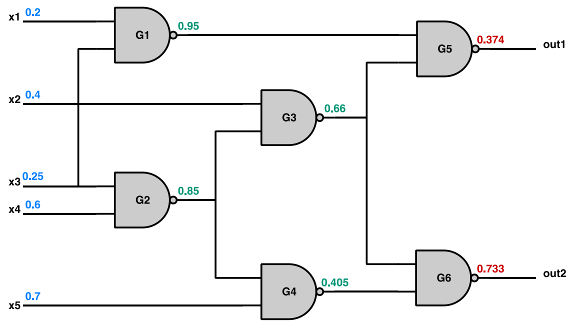
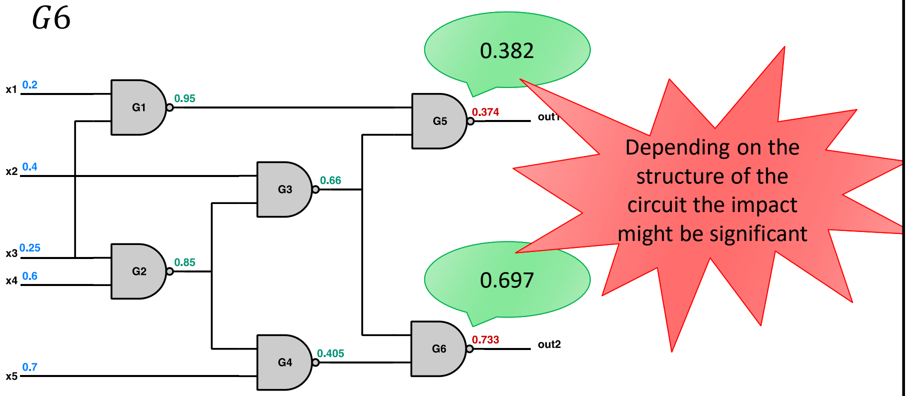
Reconvergence

- In the circuit of the figure:
  - **Reconvergence #1**: Gate $G5$ is a reconvergent node
    - There is a signal correlation with the primary input $x3$ among its inputs
  - **Reconvergence #2**: Gate $G6$ is a reconvergent node
    - There is a signal correlation with the output gate pin of $G2$ among its inputs

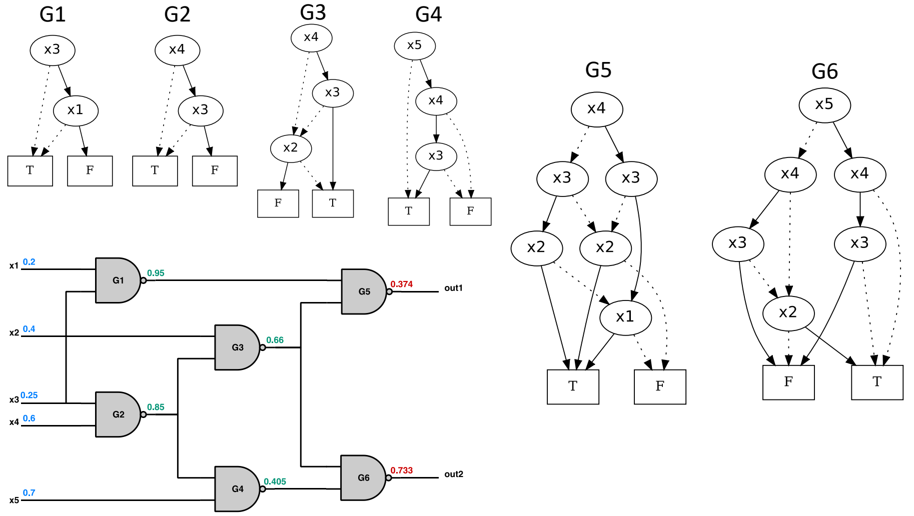


Reconvergence

- Considering the signal correlations at the gates $G5$ and $G6$



Handling of Reconvergence
Binary Decision Diagrams

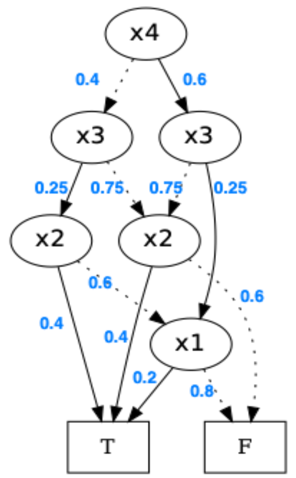


Handling of Reconvergence
Binary Decision Diagrams

- Each edge of the BDD is assigned a static probability
  - The static probability of the parent node
    - ‘1’ edge → $P_1(Gi)$
    - ‘0’ edge → $P_0(Gi)$
- Static Probability Computation for a gate
  - Traverse all the paths to the ‘1’ sink
    - Compute the product of the static probabilities of the edges across a path
    - Sum the computed products for all paths to ‘1’

Handling of Reconvergence Example

- Paths to ‘1’:
  - $x4' \rightarrow x3 \rightarrow x2$
    - $P_a = P_0(x4) \times P_1(x3) \times P_1(x2) = 0.04$
  - $x4' \rightarrow x3 \rightarrow x2' \rightarrow x1$
    - $P_b = P_0(x4) \times P_1(x3) \times P_0(x2) \times P_1(x1) = 0.012$
  - $x4' \rightarrow x3' \rightarrow x2$
    - $P_c = P_0(x4) \times P_0(x3) \times P_1(x2) = 0.12$
  - $x4 \rightarrow x3' \rightarrow x2$
    - $P_d = P_1(x4) \times P_0(x3) \times P_1(x2) = 0.18$
  - $x4 \rightarrow x3 \rightarrow x1$
    - $P_e = P_1(x4) \times P_1(x3) \times P_1(x1) = 0.03$
- Total:
  - $P_1(G5|out) = P_a + P_b + P_c + P_d + P_e = 0.382$



Not optimal way to compute it!!!